Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) An electronic semiconductor device, comprising:

a body of semiconductor material having an upper surface;

a dielectric layer extending on top of said body; and

a contact structure in said dielectric layer, said contact structure comprising a first conducting region and a second conducting region, said second conducting region being of chalcogenic material and being in electric contact with said first conducting region;

wherein said first conducting region has a longitudinal ~~direction~~ dimension delimited by an end face extending transversely to said upper surface and the longitudinal dimension and ~~forming a contact area with~~contacting said second conducting region at a contact area, the end face having width and height dimensions that are smaller than the longitudinal dimension.

2. (Original) A device according to claim 1 wherein said first conducting region extends in a direction parallel to said upper surface.

3. (Original) A device according to claim 1 wherein said end face is perpendicular to said upper surface within process tolerances.

4. (Original) A device according to claim 1 wherein said end face has a generally rectangular shape having a height and a width.

5. (Original) A device according to claim 4 wherein said height is comprised between 5 nm and 50 nm and said width is comprised between 5 nm and 50 nm.

6. (Original) A device according to claim 1, wherein the contact structure is part of a PCM storage element of a PCM memory cell that further includes a selection element, said storage element being formed by a heater element including said first conducting region and a storage region comprising said second conducting region.

7. (Original) A device according to claim 6 wherein said selection element is formed in said body, a lower electrode extends in said dielectric layer between said selection element and said first conducting region and an upper electrode extends in said dielectric layer on said second conducting region and forms a bit line.

8. (Original) A device according to claim 7 wherein said second conducting region has a reduced area portion in contact with said first conducting region and an upper enlarged portion extending on top of said reduced area portion and in contact with said upper electrode.

9. – 15. (Canceled)

16. (Currently Amended) An electronic PCM device, comprising:

a body of semiconductor material having a lower surface;

a dielectric layer extending on top of the body; and

a PCM memory cell that includes a PCM storage element formed in the dielectric layer and a selection element, the storage element being formed by a heater element and a storage region, the storage region being of chalcogenic material and being in electric contact with the heater element, wherein the heater element has an end face extending transversely to the lower surface and forming a contact area with the storage region, wherein the selection element is formed in the body, a lower electrode extends in the dielectric layer between the selection element and the heater element and an upper electrode extends in the dielectric layer on the storage region and forms a bit line.

17. (Original) The PCM device of claim 16 wherein the heater element extends longitudinally in a direction parallel to the lower surface.

18. (Original) The PCM device of claim 16 wherein the end face is perpendicular to the lower surface within process tolerances.

19. (Original) The PCM device of claim 16 wherein the end face has a generally rectangular shape having a height and a width.

20. (Original) The PCM device of claim 19 wherein the height is comprised between 5 nm and 50 nm and the width is comprised between 5 nm and 50 nm.

21. (Canceled)

22. (Currently Amended) The PCM device of claim ~~21~~ 16 wherein the storage region has a reduced area portion in contact with the heater element and an upper enlarged portion extending on top of the reduced area portion and in contact with the upper electrode.

23. (Previously Presented) The PCM device of claim 16 wherein the dielectric layer includes a plurality of dielectric layers formed on top of one another.

24. (Previously Presented) The PCM device of claim 1 wherein the dielectric layer includes a plurality of dielectric layers formed on top of one another.

25. (Currently Amended) An electronic semiconductor device, comprising:

a semiconductor body having an upper surface;

a dielectric layer positioned above the semiconductor body; and

a contact structure positioned at least partially in the dielectric layer and including a first conducting region and a second conducting region, the second conducting region being of

chalcogenic material, the first conducting region having a contact surface that contacts the second conducting region and extends transversely to the upper surface, wherein the contact surface has a generally rectangular shape having a height and a width, wherein the height is comprised between 5 nm and 50 nm and the width is comprised between 5 nm and 50 nm.

26. (Previously Presented) The device of claim 25 wherein the first conducting region extends lengthwise in a direction parallel to the upper surface.

27. (Canceled)

28. (Previously Presented) The device of claim 25, wherein the contact structure is part of a PCM storage element of a PCM memory cell that further includes a selection element, the storage element being formed by a heater element including the first conducting region and a storage region including the second conducting region.

29. (Previously Presented) The device of claim 28 wherein the selection element is formed in the body, a lower electrode extends in the dielectric layer between the selection element and the first conducting region.

30. (Previously Presented) The device of claim 25, further comprising a conductive contact extending upwardly from the upper surface of the semiconductor body, the conductive contact being electrically coupled to the first conducting region.

31. (New) An electronic semiconductor device, comprising:

a body of semiconductor material having an upper surface;

a dielectric layer extending on top of the body; and

a contact structure in the dielectric layer, the contact structure comprising a first conducting region and a second conducting region, the second conducting region being of chalcogenic material and being in electric contact with the first conducting region;

wherein the first conducting region has a longitudinal direction delimited by an end face extending transversely to the upper surface and contacting a side wall of the second conducting region, the end face having a width smaller than a corresponding width of the side wall of the second conducting region and a height smaller than a corresponding height of the side wall of the second conducting region.

32. (New) The device of claim 31 wherein the first conducting region extends in a direction parallel to the upper surface.

33. (New) The device of claim 31 wherein the height and width of the end face are each comprised between 5 nm and 50 nm.

34. (New) The device of claim 31, wherein the contact structure is part of a PCM storage element of a PCM memory cell that further includes a selection element, the storage element being formed by a heater element including the first conducting region and a storage region comprising the second conducting region.

35. (New) The device of claim 34 wherein the selection element is formed in the body, a lower electrode extends in the dielectric layer between the selection element and the first conducting region and an upper electrode extends in the dielectric layer on the second conducting region and forms a bit line.

36. (New) The device of claim 35 wherein the second conducting region has a reduced area portion in contact with the first conducting region and an upper enlarged portion extending on top of the reduced area portion and in contact with the upper electrode.

37. (New) The device of claim 31 wherein the first conducting region contacts the second conduction region only with the end face of the first conducting region.

38. (New) The device of claim 1 wherein the first conducting region contacts the second conduction region only with the end face of the first conducting region.